

## CLAIMS

- 1 1. In a circuit comprising a plurality of SOI devices wherein each of the  
2 plurality of SOI devices has a body, a mechanism for enhancing the  
3 performance of the circuit, the mechanism comprising:  
4 a circuit component for discharging accumulated electrical potential from  
5 the body of the plurality of SOI devices.
- 1 2. The mechanism of claim 1 wherein the circuit component comprises a  
2 pulse discharge circuit.
- 1 3. The mechanism of claim 1 wherein the circuit component comprises a  
2 connection to ground for at least one of the bodies of the SOI devices.
- 1 4. The mechanism of claim 2 wherein the pulse discharge circuit comprises:  
2 an input signal;  
3 a delay element coupled to the input signal; and  
4 an output signal coupled to the input signal, the output signal driving the  
5 circuit.

1 5. The mechanism of claim 2 wherein the pulse discharge circuit further  
2 comprises a pulse generator.

1 6. In a circuit comprising at least one SOI device, a method for enhancing the  
2 performance of the circuit, the method comprising the steps of:  
3 providing a pulse discharge circuit connected to the at least one SOI  
4 device;  
5 using the pulse discharge circuit to discharge any accumulated potential on  
6 the at least one SOI device prior to accessing the at least one SOI device.

1 7. The method of claim 6 wherein the circuit comprises a memory circuit.

1 8. The method of claim 6 wherein the pulse discharge circuit comprises:  
2 an input signal;  
3 a delay element coupled to the input signal; and  
4 an output signal coupled to the input signal, the output signal driving the  
5 circuit.

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1 9. In a circuit comprising a plurality of SOI devices wherein each of the  
2 plurality of SOI devices has a body, a method for enhancing the  
3 performance of the circuit, the method comprising the step of:  
4 selecting grounding the body of at least one of the plurality of SOI devices  
5 to dissipate electric potential.

1 10. The circuit of claim 9 wherein the plurality of SOI devices comprises a  
2 memory circuit.

1 11. In a circuit comprising a plurality of SOI devices wherein each of the  
2 plurality of SOI devices has a body, a method for enhancing the  
3 performance of the circuit, the method comprising the step of:  
4 providing a pulse discharge circuit, the pulse discharge circuit having a  
5 pulse generator and the pulse generator being connected to the circuit;  
6 using the pulse generator to generate a pulse;  
7 discharging any accumulated potential on the body of at least one of the  
8 plurality of SOI devices by supplying the pulse from the pulse generator to  
9 the body of the at least one of the plurality of the SOI devices at a pre-  
10 determined time.

1 12. The method of claim 11 wherein the plurality of SOI devices comprises a  
2 memory circuit.

1 13. The method of claim 12 wherein the pre-determined time is just prior to  
2 accessing the memory circuit for reading or writing data.

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